60 GHz High-Efficiency HEMT MMIC Chip Set Development for High-Power Solid State Power Amplifier

Y. Hwang, J. Lester, G. Schreyer, G. Zell, S. Schrier, D. Yamauchi,
G. Onak, B. Kasody, R.Kono, Y. C. Chen, and R. Lai

TRW Inc., Electronic Systems and Technology Division
One Space Park, Redondo Beach, CA 90278

ABSTRACT

A 60 GHz high-efficiency HEMT MMIC chip set was developed including two fully-matched HEMT MMIC chips. A 2-mil thick MMIC with 300 mW output power, 22% efficiency and a 4-mil thick gain stage MMIC. They were used as building blocks of high power (1 to 50 watts) SSPA.

INTRODUCTION

The high-efficiency broadband power amplifier is a critical unit for communication applications [1-10]. To address the V-band high power (1 to 50 watts) SSPA (Solid State Power Amplifier) requirements, a 60 GHz high-efficiency HEMT MMIC chip set was developed including two fully-matched (50 ohm input and output) HEMT MMIC chips. An output stage 2-mil thick MMIC achieves 300 mW output power with 22% efficiency and a gain stage 4-mil thick MMIC achieves 18 dBm output power with 16% efficiency. These two MMIC chips can be used as building blocks of V-band high power SSPA.

Figure 1 shows the block diagram of a broadband (59 to 64 GHz) 50 watt (47.6 dBm) SSPA. To address this broadband 50 watt SSPA requirement, a 1/4 watt output stage 2-mil thick MMIC chip and a 18 dBm gain stage 4-mil thick MMIC chip were used as building blocks of SSPA modules. The design goal of this SSPA is to achieve more than 50 watt output power and better than 60 dB gain with input power of -16 dBm.

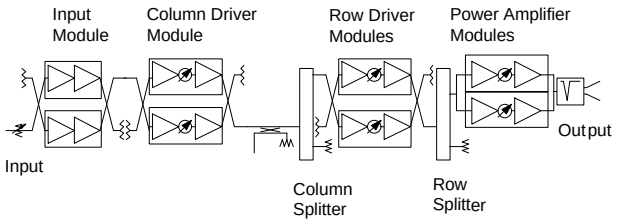

Figure 1. Block diagram of a 50 watt SSPA.

2-MIL AND 4-MIL HEMT MMIC PROCESS DESCRIPTION

The front side 0.15 µm HEMT process used for V-band power MMICs is the same as our previously reported high yield V-band power MMIC production process [1-3] with the baseline double hetero structure $In_{0.22}Ga_{0.78}As$/AlGaAs/ GaAs HEMT device profile. 750Å silicon nitride is deposited using PECVD for device passivation. The key change in the process is the fabrication of the devices and circuits on 2-mil (50 µm) thick GaAs substrates (2-mil process) compared to our previously reported 4-mil (100 µm) thick GaAs substrate baseline.

The 2-mil process has demonstrated several advantages that are crucial to achieve higher power, higher efficiency device and MMIC performance at 60 GHz. First, the thinner substrate reduces the size of the source ground via holes formed by reactive ion etching (RIE) by 50% which reduces the device source inductance. Second, the thinner substrate decreases the thermal resistance of the device by as much as 30% which results in a lower channel operating temperature. Also, the smaller via hole size allowed ground vias to be placed on every source pad (previous 4-mil thick GaAs device designs have 4 or 8

0-7803-4603-6/97/$5.00 (c) IEEE

fingers between ground source pads). The greater number of ground vias reduces the device source inductance and channel operating temperature further. A total of 3.5 µm thick gold was sputtered and plated on the backside of the wafer.

V-BAND 2-MIL THICK 1/4 WATT MMIC CHIP DESIGN AND TEST DATA

This MMIC chip uses 0.15 µm pseudomorphic InGaAs T-gate power HEMT. It is a single-ended two-stage design with the driver stage using a 0.4 mm HEMT, followed by a 0.8 mm HEMT in the output stage. It receives 13 dBm V-band signals from a preamplifier and provides 1/4 watt output power. Figure 1 shows the chip photo of this V-band 1/4 watt fully matched MMIC amplifier, APH171C. The Chip size is 4.1 mm x 1.6 mm. Thin substrate (2-mil) is selected to improve via-hole inductance, amplifier gain, and efficiency and to lower thermal resistance. The matching networks include microstrip lines of different width. MIM capacitors are used for dc block and RF bypass. EM simulation of matching structure has been performed to achieve good agreement between simulation and measurement results.

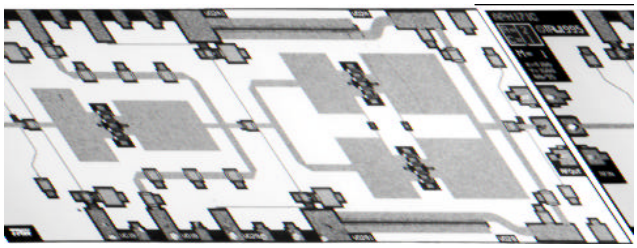

Figure 2. Chip Photo of APH171C.

The small signal s-parameters of this MMIC amplifier were tested on-wafer from 55 to 67 GHz. There is good agreement between measured and simulated small signal gain. Figure 3 shows good repeatability of measured small signal gain from 55 to 67 GHz. Figure 4 shows the gain distribution of APH171C from one wafer. The on-wafer pulsed large signal power gain of this chip was measured from 59 to 64 GHz. Figure 5 shows pulsed power gain distribution on one wafer of APH171C at 64 GHz. Some MMIC chips were mounted in V-band test fixtures for large signal test. The amplifier gain, output power and efficiency of this chip at 60 GHz were measured with input power varying from -5 to 15 dBm. At 60 GHz, it provides 17.5 dB small signal gain. At large signal operation Pin = 15 dBm, it provides 9.7 dB gain, 24.7 dBm output power and 22.5% efficiency. The device was biased at Vd=4.5V, Id1=94mA and Id2=164mA. A bandwidth of 4 GHz and less than 0.5 dB gain variation vs. frequency were achieved.

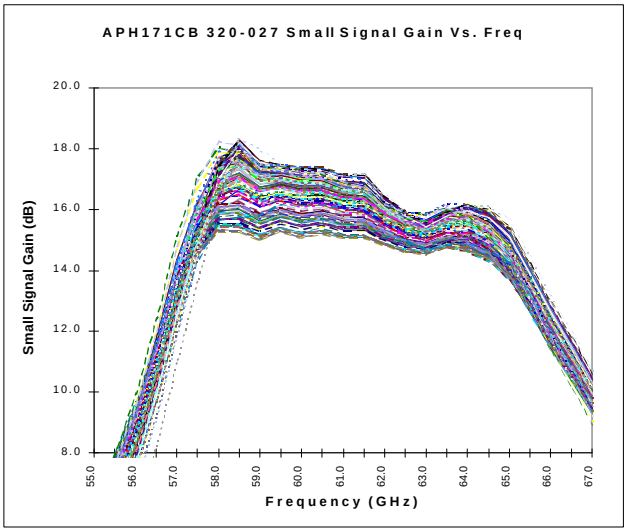

Figure 3. Measured small signal gain of APH171C from 55 to 67 GHz.

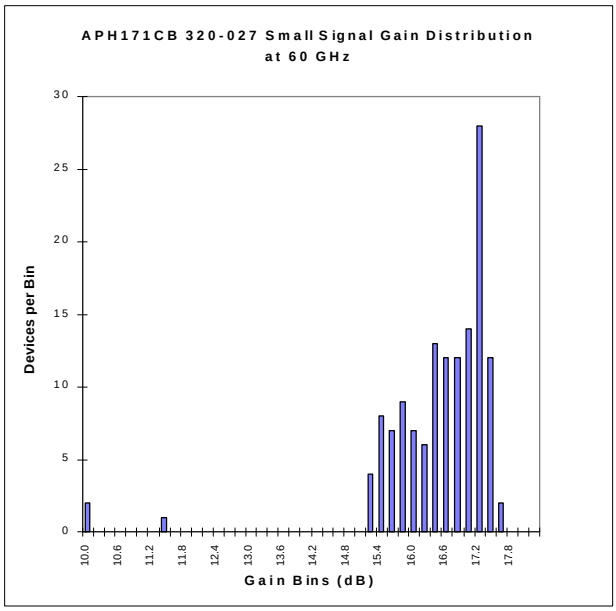

Figure 4. Small signal gain distribution of APH171C at 60 GHz.

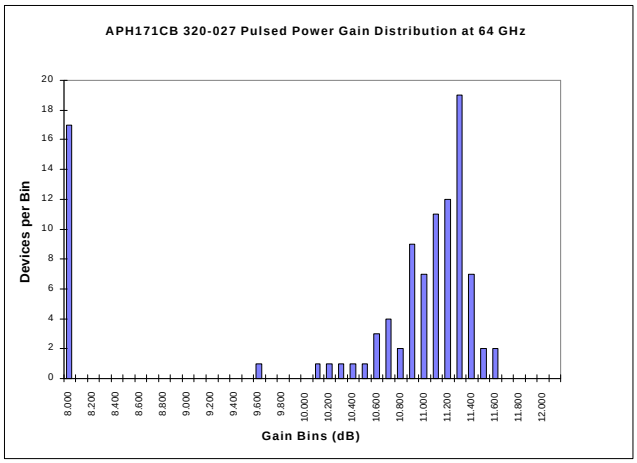

Figure 5. Pulsed power gain distribution of APH171C at 64 GHz (Pin = +13 dBm).

V-BAND 4-MIL GAIN STAGE MMIC CHIP DESIGN AND TEST DATA

This MMIC chip uses 0.15 µm pseudomorphic InGaAs T-gate power HEMT. It is a balanced two-stage design with the driver stage using a 0.06 mm HEMT, followed by a 0.1 mm HEMT in the output stage. This MMIC chip size is 3 mm x 2.5 mm. A 4-mil thick substrate was selected to provide good yield and ease of process. The matching networks include microstrip lines of different width. MIM capacitors are used for dc block and RF bypass. Lange couplers are used to achieve good input and output return loss.

Figure 6 shows measured small signal gain of this MMIC chip from 59 to 65 GHz. The small signal gain is typically greater than 13 dB. Some MMIC chips were mounted in V-band test fixtures for large signal test. The amplifier gain, output power and efficiency of this chip at 60 GHz were measured with input power varying from -5 to 10 dBm as shown in Figure 7. At 60 GHz, it provides 13.5 dB small signal gain. At large signal operation (Pin=10 dBm), it provides 8.4 dB gain, 18.4dBm output power and 16% efficiency. Device was biased at Vd=4.5V, Id=100mA. A bandwidth of 4 GHz and less than 0.5 dB gain variation vs. frequency were achieved.

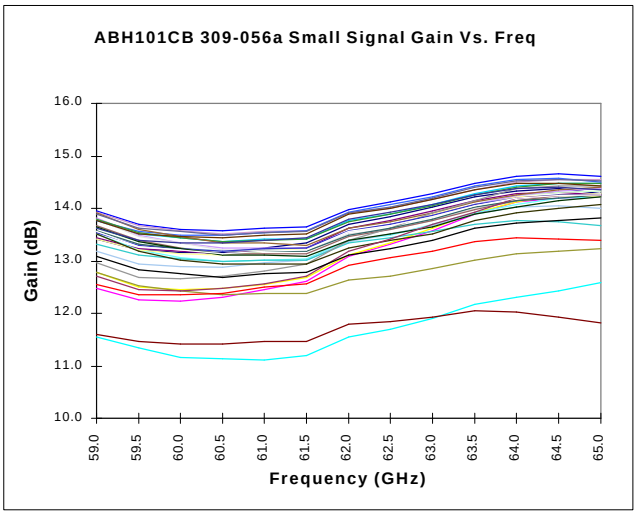

Figure 6. Measured small signal gain of ABH101CB from 59 to 65 GHz.

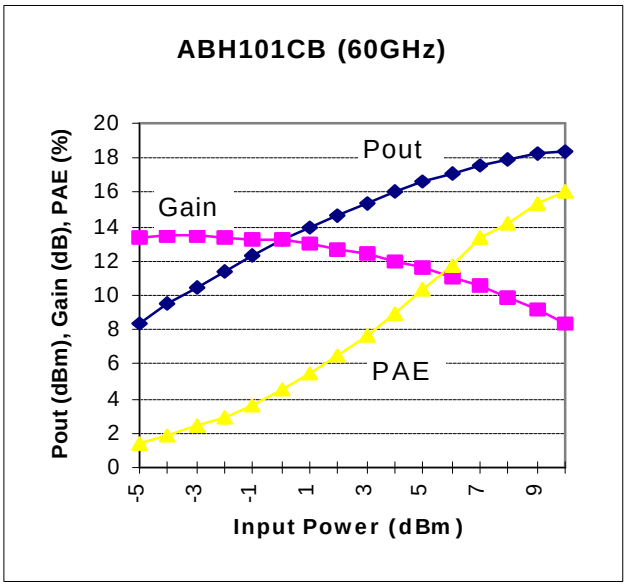

Figure 7. Measured output power, gain and efficiency vs. input power of ABH101CB at 60 GHz.

SUMMARY

We have presented V-band 2-mil and 4-mil power amplifiers using T-gate power HEMT MMIC process. A 2-mil thick MMIC with 300 mW output power, 22% efficiency and a 4-mil thick gain stage MMIC. They were used as building blocks of high power (1 to 50 watts) SSPA. These represent state-of-the-art performance of the monolithic power amplifier at this frequency. MMIC insertion of these chips into

V-band transmitter will enhance system reliability, and reduce size and weight due to its high efficiency and low thermal resistance.

ACKNOWLEDGMENTS

The authors would like to acknowledge B. Nguyen and T. Trinh for their circuit layout support, and thank Ed Rezek, Y.Y. Tu, M. Hoppe, K. Tan, M. Aust, P.D. Chow, and M. Huang for their support and guidance. We would also like to thank members of the RF Product Center and GaAs Manufacturing Line for their contributions. The results published here were supported by SSTA project.

REFERENCES

[1] R. Lai, M. Nishimoto, Y. Hwang, M. Biedenbender, B. Kasody, C. Geiger, Y. C. Chen and G. Zell, "A High Efficiency 0.15 µm 2-mil thick InGaAs/AlGaAs/GaAs V-band Power HEMT MMIC," 1996 GaAs IC Symposium Technical Digest, pp. 225-227, November 1996.

[2] Y. Hwang, G. Zell, I. Stone, G. Onak, G. Schreyer, S. Schrier, D. Yamauchi, B. Kasody, M. Nishimoto, Y. C. Chen, and R. Lai, "High Efficiency V-band MMIC Solid State Power Amplifiers," 1997 Government Microcircuit Applications Conference, March 1997.

[3] R. Lai et al., "0.15 µm InGaAs/AlGaAs/GaAs HEMT Production Process for High Performance and High Yield V-Band Power MMICs", 1995 GaAs IC Symposium Tech. Digest, San Diego CA, pp. 105-108.

[4] S. Chen, P. M. Smith, S. J. Liu, W. F. Kopp, and T. J. Rogers, "A 60-GHz High Efficiency Monolithic Power Amplifier Using 0.1-µm PHEMT," IEEE Microwave and Guided Wave Letters, Vol. 5, no. 6, pp. 201-203, June 1995.

[5] R. Lai et al., "High Power 0.15 µm V-Band Pseudomorphic InGaAs/AlGaAs/GaAs HEMT", IEEE Microwave and Guided Letters, Vol. 3, p. 363, Oct. 1993.

[6] C.H. Chen et. al, "Reliability Study on Pseudomorphic InGaAs Power HEMT Devices at 60GHz," IEEE MTT Symposium Digest, San Diego, CA, p. 817, 1994.

[7] C.H. Chen et. al, "RF-Stressed Life Test of Pseudomorphic InGaAs Power HEMT MMIC at 44GHz," IEEE MTT Symposium Digest, Orlando, FL, p. 713, 1995.

[8] C. K. Pao et al., "V-Band High Efficiency Monolithic Pseudomorphic HEMT Power Amplifiers," IEEE Microwave and Guided Wave Letters, Vol. 2, no. 10, pp. 394-396, Oct. 1992.

[9] R. E. Kasody et al., "A High Efficiency V-Band Monolithic HEMT Power Amplifier," IEEE Microwave and Guided Wave Letters, Vol. 4, no. 9, Sept. 1994.

[10] M. Biedenbender et al., "A Power HEMT Production Process for High Efficiency Ka-Band MMIC Power Amplifiers", 1993 GaAs IC Symposium Tech. Digest, San Jose, CA.